EXHIBIT 3

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Hyun Lee
App. No.	:	13/288,850
Filed	:	November 3, 2011
For	:	ARCHITECTURE FOR MEMORY MODULE WITH PACKAGES OF THREE-DIMENSIONAL STACKED (3DS) MEMORY CHIPS
Examiner	:	ZARABIAN, AMIR
Art Unit	:	2827
Conf. No.	:	2466
Docket No.	:	NETL.071A

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/Jamie J. Zheng/

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AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Non-Final Office Action dated October 11, 2013 for the above-identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

AMENDMENTS to the CLAIMS begin on Page 2 of this paper.

REMARKS begin on Page 9 of this paper.

IN THE CLAIMS:

Rewrite the pending claims as follows:

1. (**Previously Presented**) A memory package, comprising:

a plurality of input/output terminals via which the memory package communicate data and control/address signals with one or more external devices;

a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports;

at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

a control die comprising at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, and at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal, the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.

2. (**Previously Presented**) The memory package of claim 1, wherein the control signals include data path control signals for controlling the first and second data conduits.

3. (**Previously Presented**) The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals.

4. (**Previously Presented**) The memory package of claim 3, wherein the control signals include command/address signals and wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies.

5. (**Cancelled**)

REMARKS

This amendment responds to the Non-Final Office Action dated October 11, 2013. In the Office Action, the Examiner:

- withdrew the restriction requirement of claims 29-34;
- noted two issues with the Information Disclosure Statement submitted on 5/23/2012;
- objected to informalities in claim 5 and claim 8;
- rejected claim 5 under 35 U.S.C. 112(b) or 35 U.S.C.112 (pre-AIA), second paragraph as being indefinite;
- rejected claims 1-4, 7, 9-13, 15-21, 23, 24, 27-29, 31, 33, and 34 under pre-AIA 35 U.S.C. 102(b) as being anticipated by Rajan et al. (US 2008/0025137);
- rejected claims 6, 14, 25, and 26 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Rajan in view of Kirby et al. (US 2011/0193226);
- rejected claims 30 and 32 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Rajan in view of Gervasi (US 2006/0259678); and
- objected to claims 8 and 22 as being dependent upon a rejected base claim.

Applicant appreciates the allowance of claims 8 and 22 if rewritten in independent form, but would like to request reconsideration of the rejected claims in light of the amendments and remarks.

I. CLAIM AMENDMENT

Claims 5, 9 and 10 are cancelled. Claims 8, 15-19 and 32 are amended. New claims 35-37 are presented. No new matter is added.

II. INFORMATION DISCLOSURE STATEMENT SUBMITTED ON 5/23/2012

The Examiner noted that the document "A Quantitative Analysis of Performance Benefits of 3D Die Stacking on Mobile and Embedded SoC" in the information statement filed 05/23/2012 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because a date has not been provided. Base on a recent Internet search, this article appears to have been published in 978-3-9810801-7-9/DATE11/●2011 EDAA (http://www.date-

conference.com/proceedings/PAPERS/2011/DATE11/PDFFILES/10.7_4.PDF). So, the year of publication is 2011. The exact date of this publication, however, is unknown to the Applicant.

III. OBJECTION TO INFORMALITIES IN CLAIM 5 AND CLAIM 8

Claim 5 is cancelled. Claim 8 is amended to cure the informalities. Therefore, the objection to claim 5 is moot and the objection to claim 8 should be withdrawn.

IV. REJECTION OF CLAIM 5 UNDER 35 U.S.C. 112(B) OR 35 U.S.C.112 (PRE-AIA), SECOND PARAGRAPH

Claim 5 is cancelled. Therefore, the rejection thereof is moot.

V. REJECTION OF CLAIMS 1-4, 7, 9-13, 15-21, 23, 24, 27-29, 31, 33, AND 34 UNDER PRE-AIA 35 U.S.C. 102(B) AS BEING ANTICIPATED BY RAJAN ET AL. (US 2008/0025137)

Claim 1 recites:

> A memory package, comprising:
> a plurality of input/output terminals via which the memory package communicate data and control/address signals with one or more external devices;
> a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports;
> at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
> a control die comprising at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, and at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal, the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.

First of all, Rajan does not disclose "a plurality of stacked array dies." Rajan merely stacks DRAM circuits 206A-D, which are different from array dies. As a result, Rajan's buffer chip 202 also operates very differently from the control die in claim 1. In rejecting claim 1, the Examiner states that Rajan (FIG. 2B) shows a memory package as recited in

claim 1. The Examiner further cites Paragraph [0044] as disclosing the control die as recited in claim 1. Paragraph [0044] in Rajan, however, merely states:

> As shown in each of such figures, the buffer chip 202 is placed electrically between an electronic host system 204 and a stack of DRAM circuits 206A-D. In the context of the present description, a stack may refer to any collection of memory circuits. Further, the buffer chip 202 may include any device capable of buffering a stack of circuits (e.g. DRAM circuits 206A-D, etc.). Specifically, the buffer chip 202 may be capable of buffering the stack of DRAM circuits 206A-D to electrically and/or logically resemble at least one larger capacity DRAM circuit to the host system 204. In this way, the stack of DRAM circuits 206A-D may appear as a smaller quantity of larger capacity DRAM circuits to the host system 204.

Thus, the statements in this paragraph [0044] of Rajan says nothing about the existence of a first data conduit and a second data conduit in the buffer chip 202 and "a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals." According to this paragraph [0044], all that is required of the buffer chip 202 is the capability of buffering the stack of DRAM circuits 206A-D to electrically and/or logically resemble at least one larger capacity DRAM circuit to the host system, and this requirement does not necessitate the use of a first data conduit and a second data conduit in the buffer chip 202 and "a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals."

Furthermore, according to paragraphs [0043] and [0044], this same capability of buffering the stack of DRAM circuits 206A-D to electrically and/or logically resemble at least one larger capacity DRAM circuit to the host system is required for each of the FIGS. 2A-2E, which show various configurations of a buffered stack of DRAM circuits 206A-D with the buffer chip 202. Since FIG. 2D of Rajan shows a single data bus between the buffer chip and all of the stacked DRAM circuits 206A-D (*Rajan, paragraph [0051]*), this capability of buffering the stack of DRAM circuits 206A-D, which also applies to the configuration in FIG. 2D, can not be said to imply the existence of first and second data conduits in the buffer chip 202 and a control circuit controlling the respective states of the first data conduit and the second data conduit in response to any received control signals, because the first and second data conduits would be coupled to a same data line in the single data bus in FIG. 2D and it would make no sense to try to control respective states or the first data conduit and the second data conduit.

Therefore, Rajan fails to disclose each and every limitation in claim 1, and claim 1 is patentable over Rajan.

Claims 2-4 and 7 depend from claim 1 and include further limitations in addition to the limitations in claim 1. Therefore, claims 2-4 and 7 are patentable for at least the same reasons claim 1 is patentable.

Claims 2-4 and 7 are also patentable for the additional features recited therein. For example, claim 2 includes the further limitations that the control signals received via the one or more second terminals of the plurality of terminals include data path control signals for controlling the first and second data conduits. Rajan does not disclose any data path control signals. In Rajan, besides the data signals, the signals the buffer chip receives are address/control/clock signals (*Rajan, Paragraph [0025]*). These are signals used for memory operations, not for controlling any data conduits in the buffer chip 202.

As a further example, claim 3 recites "the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals." As stated above, Rajan does not disclose any data path control signals. Therefore, Rajan cannot be said to disclose anything about generating the data path control signals in its buffer chip 202.

Claims 9-10 are cancelled. Therefore, the rejections thereof are moot.

The arguments regarding claim 1 applies to claim 11. Therefore, claim 11 is also patentable over Rajan.

Claims 12-13, and claims 15-19 as amended depend from claim 11 and include further limitations in addition to the limitations in claim 11. Therefore, claims 12-13, and claims 15-19 as amended are patentable for at least the same reasons claim 11 is patentable.

Claims 12-13, and claims 15-19 as amended are also patentable for the additional features recited therein. For example, claim 15 is amended to include certain features in claim 22, which are considered allowable.

Claim 16 as amended recites that the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and wherein the chip select signal is generated using at least one address signal in the